

IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 8, 29, 35, and 37. These sheets, which include Figs. 7 and 8, 28 and 29, 35, and 37, replace the original sheets including Figs. 7 and 8, 28 and 29, and 35 and 37.

Attachment: Replacement Sheets (4 sheets)

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 7-12, 14, and 21-33 are pending in the present application. Claims 1, 11, 12, 14, 21, 22, 30, and 32 are amended and Claims 2-6, 13, and 15-20 are canceled without prejudice by the present amendment.

In the outstanding Office Action, the drawings were objected to; Claims 1-33 were rejected under 35 U.S.C. § 112, first paragraph; and Claims 1-33 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tran et al. (U.S. Patent No. 6,577,549, herein "Tran").

Regarding the objection to the drawings, Figures 8, 29, 35, and 37 are amended without adding new matter. More specifically, Figure 8 is amended to replace the term "low" with "high" and vice versa, consistent with the specification at page 30, lines 20-23; Figure 29 is amended to add the reference term "Vtemp"; and Figures 35 and 37 are amended to show the "L" and the "H" levels for Vtemp1 and Vtemp2 signals on separate graphs.

In addition, Applicants respectfully submit that the reference characters indicated in the outstanding Office Action in numbered paragraph 1 as not mentioned in the description are disclosed in the specification. More specifically, Applicants respectfully submit that those characters are present in the specification as follows:

- a) Regarding elements 32 in FIG. 3, metal wiring layer 32 is disclosed on page 24, line 9.
- b) MC00 to MC23 in FIG. 2 are disclosed at page 20, lines 3-5 and at page 28, lines 17 and 21.
- c) STI in FIG. 4 is the element isolation region indicated on page 22, lines 17-18.
- d) Dimensions h1, h2, w1, and w2 shown in FIG. 5 are disclosed on page 35, lines 26-27 and page 36, lines 4-5.

e) Regarding all the elements in FIG. 8, it is disclosed on page 30, lines 15-20 that FIG. 8 shows the intensity of the magnetic field using two dimensional contour lines. Also, it is apparent from FIG. 8 that H1 to H12 indicate the level of magnetic field intensity.

f) The write area and the non-write area shown in FIGS. 9-11 and 14-16 are disclosed on page 31, line 25 to page 32, line 4. The write area of the drawings is an area satisfying the equation indicated on page 31, line 27, wherein data is written using H_x and H_y of this area.

g) Line path in FIG. 13 is "line path I" indicated on page 35, line 16.

h) Regarding (W10), (W11), (W12), I10, I11, Isource, B, C and D in FIG. 19, the specification discloses those reference signals at page 48, lines 17-19 for B; page 49, lines 7-18 for I11, (W10), C and D; and at page 50, lines 6-17 for I10, (W11), (W12) and Isource.

i) Regarding the write area in FIG. 21, it is disclosed on page 52, line 4 that FIG. 21 shows an asteroid curve. Therefore, the write area in FIG. 21 is defined in the same way as the write area in FIG. 9 indicated above.

j) Regarding all the elements in FIGS. 25, 27, 30, 33, 35, 37, 53-58 and 69-70, the specification discloses the following:

on page 58, lines 11 to page 59, line 6 that FIG. 25 shows currents I10, I11 and I12 and Isource in FIG. 24.

FIG. 27 relates to the modification of the fourth embodiment as indicated on page 11, lines 16-20. Thus, currents I10, I11 and I12 and Isource in FIG. 27 are the same as currents I10, I11 and I12 and Isource in FIG. 26.

on page 64, lines 20-25 that FIG. 30 shows signal Vtemp and currents I13-I15 in FIGS. 28 and 29.

on page 68, lines 7-11 that FIG. 33 shows signal Vtemp and currents I13-I15 in FIG. 32.

on page 71, lines 22-26 that FIG. 35 shows signals Vtemp1 and Vtemp2 and currents I20-I24 in FIG. 34.

on page 74, line 24 to page 75, line 2 that FIG. 37 shows signals Vtemp1 and Vtemp2 and currents I20-I24 in FIG. 36.

on page 108, lines 16-23 that FIG. 53 is the block diagram of a memory cell array.

on page 108, line 23 to page 109, line 5 that FIG. 54 shows data to be written into memory cells MC00 - MC44.

P1-P7 and AREA1 - AREA6 shown in FIG. 55 are disclosed on page 113, line 14 to page 114, line 10.

FIG. 56 shows the same AREA1 - AREA6 as shown in FIG. 55.

In FIG. 57, the areas indicated by broken lines correspond to AREA6 shown in FIGS. 55 and 56. AREA6 change with temperature as disclosed on page 115, lines 4-10.

Steps S30-S34 shown in FIG. 58 are disclosed on page 116, line 1 to page 117, line 14.

Each of the elements shown in FIG. 69 is the same as that in FIG. 3.

FIG. 70 illustrates the same flowchart as FIG. 51, except that steps S18 and S22 are replaced with steps S40 and S41 in FIG. 70, respectively. The outcome obtained from steps S40 and S41 are disclosed on page 125, lines 18-22.

k) Regarding T3~T4, T4~T5 and all their corresponding current values in FIGs. 47-50, it is disclosed on page 96, lines 11-12 that T3~T4 and T4~T5 are temperature ranges. Also, it is disclosed on page 102, starting line 8 that each of the values in FIGs. 47-50 is write current I1 or I2 or current ratio I1/I2 which corresponds to each of the temperature ranges.

l) Write current I1 (line 13, page 52) is shown in FIGs. 5 and 6, in which write current I1 is supplied to the digit lines.

m) Write current I2 (line 15, page 52) is shown in FIGS. 5 and 6, in which write current I2 is supplied to the bit lines.

Further, the specification is amended at page 105, line 23, to remove the term "step S10." Accordingly, it is respectfully requested that this objection be withdrawn.

Regarding the rejection of Claims 1-33 under 35 U.S.C. § 112, first paragraph, it is believed that the elements indicated by the outstanding Office Action as not understood are clearly identified in the above paragraphs together with their location in the specification. Accordingly, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claims 1-33 under 35 U.S.C. § 103(a) as unpatentable over Tran, independent Claims 1, 11, 30 and 32 are amended to recite more clearly novel features that distinguish over the applied art. No new matter has been added.

More specifically, the claim amendments of Claims 1 and 30 find support in original Figures 22-38 and 41-42 in which the claimed write circuit corresponds to, for example, current sources 15 and 18 and circuits 70-1 and 70-2 shown in Figure 22. The first and second current sources of Claims 1 and 30 correspond to, for example, circuit blocks 76 and 93 shown in Figure 24. The circuit blocks 76 and 93 are controlled by signals Opt1 and Opt2, respectively, and these signals depend on temperature as disclosed in the specification at page 59, lines 16-17. In addition, the current values of currents (the first and second write currents in Claims 1 and 30) supplied from sources 15 and 18 to selectors 14 and 17, respectively, depend from the supply current of the current source 74 which includes blocks 76 and 93.

Turning to the applied art, Tran shows in Figure 3 a memory device having memory cells 130, a row decoder 56, a column decoder 54, current sources 700, and a temperature sensor 10. However, Tran does not teach or suggest (i) a write circuit that includes first and second current sources whose supply circuits have different temperature dependencies, (ii)

the first and second current sources are set to be one of an enable or disable state in accordance with an ambient temperature, and (iii) at least one of the current values of the first and second write currents is controlled in accordance with the supply currents of the first and second current sources as required by amended Claims 1 and 30.

Accordingly, it is respectfully submitted that independent Claims 1 and 30 and each of the claims depending therefrom patentably distinguish over Tran.

Regarding the amendments to Claims 11 and 32, the claimed devices find support in original Figures 41 and 42. In a non-limiting example, the write circuit in each of Claims 11 and 32 corresponds to, for example, current sources 15 and 18 and circuits 70-1 and 70-2 shown in Figure 41. The first and second MOS transistors correspond to, for example, transistors 131, 133, and 135 and transistors 138, 140, and 142 shown in Figure 41. Further, the specification discloses at page 95, lines 9-17, that transistors 131, 133, and 135 and transistors 138, 140, and 142 are controlled based on a temperature as claimed.

Tran does not teach or suggest (i) a write circuit that includes a plurality of first MOS transistors which generate a first write current and a plurality of second MOS transistors that generate a second write current, and (ii) the number of transistors to be set in an ON state is changed in accordance with an ambient temperature at least in one of the first and second MOS transistors as required by amended Claims 11 and 32.

Accordingly, it is respectfully submitted that independent Claims 11 and 32 and each of the claims depending therefrom patentably distinguish over Tran.

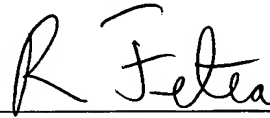
Regarding independent Claim 27, Claim 27 recites that a control method of a semiconductor memory device includes, holding in advance in a holding section optimum values of first and second write currents according to temperatures. However, Tran does not teach or suggest the above-noted feature. Accordingly, it is respectfully submitted that

independent Claim 27 and each of the claims depending therefrom patentably distinguish over Tran.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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